02-08-00 A

PTO/SB/05 (12/97)

Please type a plus sign (+) inside this box → [+]

Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	TI - 29599
First Named Inventor or Application Identifier	ROBERT STEINHOFF, ET AL.
Title	BI-DIRECTIONAL ESD PROTECTION CIRCUIT
Express Mail Label No.	EL360238881US

APPLICATION ELEMENTS

See MPEP Chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] *Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original, and a duplicate for fee processing)*
2. [X] Specification *[Total Pages 14]* *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R&D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC d113)* *[Total Sheets 4]*
4. Oath or Declaration *[Total Pages 1]*
   - a. [X] Newly Executed (original or copy)
   - b. [ ] Copy from a prior application (37 CFR §1.63(d)) *(for continuation/divisional with Box 17 completed)*

   [Note Box 5 below]

   - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c. [ ] Statement verifying identical of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & Documents(s))
9. [ ] 37 CFR §3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] *Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *if foreign priority is claimed)*
16. [ ] Other*

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information below and in a preliminary amendment:*

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: /

Prior application information: ***Examiner*** ***Group / Art Unit:***

18. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* or [X] *Correspondence address below*

NAME	ROBERT N. ROUNTREE Texas Instruments Incorporated				
ADDRESS	Mail Station 3999 P. O. Box 655474				
CITY	Dallas	*STATE*	TX	*ZIP CODE*	75265
COUNTRY	U.S.A.	*TELEPHONE*	(972) 917-4431	*FAX*	(972) 917-4418

Name (Print/Type)	ROBERT N. ROUNTREE	*Registration No. (Attorney/Agent)*	39,347
Signature	Robert N. Rountree	*Date*	2/7/00

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

BI-DIRECTIONAL ESD PROTECTION CIRCUIT

CLAIM TO PRIORITY OF PROVISIONAL APPLICATION

This application claims priority under 35 U.S.C. § 119(e)(1) of provisional application number 60/164,680, filed 11/10/99.

FIELD OF THE INVENTION

This invention relates to an integrated circuit and more particularly to a bi-directional protection circuit.

BACKGROUND OF THE INVENTION

Present complementary metal oxide semiconductor (CMOS) and bipolar-CMOS (BiCMOS) circuits employ electrostatic discharge protection (ESD) circuits to protect against electrostatic discharge due to ordinary human and machine handling. This electrostatic discharge occurs when the semiconductor circuit contacts an object that is charged to a substantially different electrostatic potential of typically several thousand volts. The contact produces a short-duration, high-current transient in the semiconductor circuit. This high current transient may damage the semiconductor circuit through joule heating. Furthermore, high voltage developed across internal components of the semiconductor circuit may damage MOS transistor gate oxide.

Sensitivity of the semiconductor circuit is determined by various test methods. A typical circuit used to determine sensitivity of the semiconductor circuit to human handling includes a capacitor and resistor that emulate a human body resistor-capacitor (RC) time constant. The capacitor is preferably 100 pF, and the resistor is preferably 1500 Ω, thereby providing a 150-nanosecond time constant. A semiconductor device is connected to the test circuit at a

predetermined external terminal for a selected test pin combination. In operation, the capacitor is initially charged to a predetermined stress voltage and discharged through the resistor and the semiconductor device. This predetermined stress voltage preferably includes both positive and negative stress voltages with respect to a reference pin or terminal. A post stress current-voltage measurement determines whether the semiconductor device is damaged. Although this test effectively emulates electrostatic discharge from a human body, it fails to comprehend other common forms of electrostatic discharge.

A charged-device ESD test is another common test method for testing semiconductor device sensitivity. This method is typically used to determine sensitivity of the semiconductor circuit to ESD under automated manufacturing conditions. The test circuit includes a stress voltage supply connected in series with a current limiting resistor. The semiconductor device forms a capacitor above a ground plane that is typically 1-2 pF. A low impedance conductor forms a discharge path having an RC time constant typically two orders of magnitude less than a human body model ESD tester. In operation, the semiconductor device is initially charged with respect to the ground plane to a predetermined stress voltage. The semiconductor device is then discharged at a selected terminal through the low impedance conductor. This connection produces a high-voltage, high-current discharge in which a magnitude of the initial voltage across the semiconductor device approaches that of the initial stress voltage.

A particular protection circuit design problem arises when protection circuits are connected to an external terminal that receives both positive and negative voltages with respect to a reference terminal such as V_{SS} during normal circuit operation. Many analog and mixed signal circuits must accommodate such positive and negative signal voltage swings. These signal voltage swings will turn on conventional transistors during normal circuit operation. These positive and negative voltage swings, therefore, preclude a use of many conventional protection circuit devices. Furthermore, the protection circuits of analog and mixed signal circuits must conduct current in a low impedance state in response to an external ESD pulse. They must also

remain in a high impedance state during normal circuit operation, and they must protect against positive and negative ESD pulses outside of normal operating parameters as well.

Referring now to FIG. 4, there is a dual silicon-controlled-rectifier (SCR) circuit of the prior art. This dual SCR circuit includes SCR circuits 406 and 408 connected between external terminal or bond pad 400 and reference terminal 410. The SCR circuits are arranged in parallel with opposite polarities. Thus, SCR 406 has an anode connected to external terminal 400 and a cathode connected to reference terminal 410 to conduct in response to positive ESD pulses at external terminal 400. SCR 408 has a cathode connected to external terminal 400 and an anode connected to reference terminal 410 to conduct in response to negative ESD pulses at external terminal 400. These circuits offer limited flexibility in adjustment of trigger voltage thresholds. They are typically activated by a PN junction avalanche threshold voltage in response to a relatively high voltage ESD pulse. This high voltage ESD pulse may damage thin oxide devices in protected circuit 404 prior to activating either SCR. These circuits have a further disadvantage that two of them are required for bi-directional operation in response to both polarities of ESD stress.

SUMMARY OF THE INVENTION

These problems are resolved by a structure with an external terminal and a reference terminal. The structure includes a first transistor formed on a substrate. The first transistor has a current path coupled between the external terminal and the reference terminal. A second transistor has a current path coupled between the external terminal and the substrate. A third transistor has a current path coupled between the substrate and the reference terminal.

The present invention provides bi-directional ESD protection for positive and negative operating voltages. Circuit area is conserved by a single primary protection device.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the invention may be gained by reading the subsequent detailed description with reference to the drawings wherein:

FIG. 1A is a schematic diagram of a protection circuit of the present invention using MOS transistors;

FIG. 1B is a layout diagram of the protection circuit of FIG. 1A;

FIG. 1C is a cross section diagram of the protection circuit of FIG. 1B taken at A-A;

FIG. 2A is a schematic diagram of another embodiment of the protection circuit of the present invention;

FIG. 2B is a layout diagram of the protection circuit of FIG. 2A;

FIG. 3 is a schematic diagram of yet another embodiment of the protection circuit of the present invention;

FIG. 4 is a schematic diagram of a bi-directional protection circuit of the prior art.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to FIG. 1A, there is a schematic diagram of a protection circuit of the present invention using a metal oxide semiconductor (MOS) transistor 106 as a primary protection device. This MOS transistor 106 has a current path connected between bond pad or external terminal 100 and reference terminal 102. A control gate of the MOS transistor 106 is coupled to a substrate or bulk terminal via lead 108. The substrate terminal is connected to a common terminal of current paths of MOS transistors 118 and 120. These MOS transistors are preferably about 30 micrometers wide for an on resistance of about 1k Ω. A resistor 114 couples another end of the current path of transistor 118 to bond pad 100. A similar resistor 116 couples another end of the current path of transistor 120 to reference terminal 102. Both these resistors 114 and 116 are preferably about 1k Ω each. A control gate of transistor 118 is connected to a common terminal of transistor 120 and resistor 116. Another control gate of transistor 120 is

connected to a common terminal of transistor 118 and resistor 114. The bond pad 100 is connected to protected circuit 188.

The layout of the protection circuit of FIG. 1A will now be explained in detail with reference to FIG. 1B and the cross section diagram of FIG. 1C at A-A. Reference numerals of these figures correspond to comparable reference numerals of FIG. 1A. The layout of FIG. 1B includes MOS transistors 106, 118 and 120 formed on P-substrate 172 within lightly doped P-well region 171. A heavily doped N+ diffusion under field (DUF) 170 underlies the P-well region 171. This DUF 170 is preferably about 4-6 micrometers thick and about 3-4 micrometers below the silicon substrate surface. The P-well region 171 is enclosed by lightly doped N-well region 104. This N-well region 104 extends from a face into the substrate to make electrical contact with the underlying DUF 170, thereby electrically isolating P-well region 171 from the rest of the P-substrate 172. The N-well region 104 indicated by the dashed line (FIG. 1A) is electrically contacted by N+ doped region 156 and overlying first metal stripe 111 designated by a dotted fill pattern. This N+ doped region is preferably 0.3-0.4 micrometers thick. The N+ doped region 156 and first metal stripe 111 are electrically connected by contact areas 158 designated by a solid fill pattern. The metal stripe 111 is preferably connected to a positive supply voltage terminal.

The MOS transistor 106 includes plural alternating drain 180 and source regions 182 with intervening control gate regions 126. Common drain and source regions are connected to respective first metal stripes 163 and 164 by contacts 160 and 162. Each first metal drain stripe is connected to a second metal bus 150 by vias 128 indicated by a cross fill pattern. The second metal bus 150 is further connected to the bond pad or external terminal 100. Each first metal source stripe is connected to a second metal bus 152 by vias 129 and to V_{SS} reference supply terminal 102. The control gate 126 of MOS transistor 106 is connected to P+ region 132 by first metal 108 and respective contacts. This P+ region 132 electrically connects the control gate 126 to the P-well region 171. First metal region 108 further connects P+ region 132 to N+ region 144 at a common current path terminal between transistors 118 and 120. The current path terminal

142 of transistor 120 is connected by first metal lead 122 to polycrystalline silicon resistor 116 and to the control gate of transistor 118. Polycrystalline silicon resistor 116 is further connected and to reference terminal 152 by lead 112. The current path terminal 140 of transistor 118 is connected by first metal lead 124 to polycrystalline silicon resistor 114 and to the control gate of transistor 120. Polycrystalline silicon resistor 114 is connected and to bond pad 150 by lead 110.

In normal circuit operation when there is no ESD pulse, the protection circuit, including MOS transistor 106, is designed to remain in a high impedance state. When a voltage at bond pad 100 is more than one MOS transistor threshold voltage (V_T) positive with respect to reference terminal 102, transistor 118 is off. The voltage at lead 124, therefore, is the same as at bond pad 100, and transistor 120 is on. In this on state, transistor 120 holds lead 108 to the voltage at reference terminal 102. Thus, transistor 106 remains off. Alternatively, when a voltage at bond pad 100 is more than one V_T negative with respect to reference terminal 102, transistor 120 is off, and transistor 118 is on. In this on state, transistor 118 holds lead 108 to the voltage at bond pad 100. Thus, transistor 106 remains off. The on-resistance of transistors 118 and 120 and respective series resistors 114 and 116 are chosen so that normal signal transitions at bond pad 100 do not capacitively couple more than a diode drop or about 0.7 volts to the common gate-substrate lead 108. In the embodiment of FIG. 1A, resistors 114 and 116 are formed from P+ doped polycrystalline silicon with a silicide blocking layer. The resistance of these resistors and the on resistance of each of transistors 118 and 120, therefore, is preferably about 1k Ω each.

During ESD operation, application of a positive ESD pulse to bond pad 100 with respect to reference terminal 102 capacitively couples a positive voltage via parasitic gate-drain capacitance (not shown) of transistor 106 to lead 108. The positive transition of lead 108 increases the voltage at P-well region 171 through P+ doped region 132. This positive voltage at leads 110 and 108 initiates a transition of the parasitic NPN bipolar transistor of MOS transistor 106 from BV_{CBO} (open emitter collector-base breakdown voltage) to BV_{CEO} (open base collector-emitter breakdown) or snapback. In snapback, MOS transistor 106, including the parasitic NPN transistor, conduct the ESD current from bond pad 100 to reference terminal 102,

thereby preventing an excessive voltage increase that might otherwise damage protected circuit 188. The ESD pulse at bond pad 100 also couples a voltage to lead 124 and turns on transistor 120. The on resistance of transistor 120 together with the series resistance of resistor 116, however, provide a relatively slow discharge of the gate capacitance of MOS transistor 106. The voltage coupled to lead 108, therefore, is not effectively discharged by transistor 120 until most of the ESD current has been discharged.

Application of a negative ESD pulse to bond pad 100 with respect to reference terminal 102 has the same effect as application of a positive ESD pulse to reference terminal 102 with respect to bond pad 100. Furthermore, due to symmetry of the circuit of FIG. 1A and isolation of the P-well region 171 from P-substrate 172, the protection circuit operates as previously described except for a change of polarity. The negative ESD pulse capacitively couples a negative voltage via parasitic gate-drain capacitance of transistor 106 to lead 108. The negative transition of lead 108 decreases the voltage at P-well region 171 through P+ doped region 132. This negative voltage at leads 110 and 108 initiates a transition of the parasitic NPN bipolar transistor of MOS transistor 106 from BV_{CBO} to BV_{CEO} or snapback. In snapback, MOS transistor 106, including the parasitic NPN transistor, conduct the ESD current from reference terminal 102 to bond pad 100. The ESD pulse at bond pad 100 also couples a negative voltage to lead 124 and turns on transistor 118. The on resistance of transistor 118 together with the series resistance of resistor 114 provide a relatively slow discharge of the gate capacitance of MOS transistor 106. The voltage coupled to lead 108, therefore, is not effectively discharged by transistor 118 until most of the ESD current has been discharged.

This circuit is highly advantageous in providing ESD protection against both positive and negative ESD stress pulses. This bi-directional operation provides this ESD protection with a single MOS transistor 106 as a primary protection device. This single device conserves layout area and minimizes circuitry adjacent the bond pad. A further advantage of the present invention is the compatibility with both positive and negative signal voltages at bond pad 100 during normal operation. For either polarity of signal voltage, the protection circuit, including MOS

transistor 106, remains in a high impedance or nonconducting state during normal circuit operation.

Referring now to FIG. 2A, there is a schematic diagram of another embodiment of the protection circuit of the present invention and a corresponding layout diagram (FIG. 2A). This embodiment is the same as the protection circuit of FIG.1A except for the addition of diodes 196 and 198. These diodes are formed by the addition of P+ heavily doped regions respectively designated 196 and 198 within N-well region 104. These diodes 196 and 198 conduct ESD current to N-well region 104 and DUF region 170 under forward bias during respective positive and negative ESD pulses at bond pad 100. For a positive ESD pulse at bond pad 100, for example, the ESD current increases a voltage at N-well region 104 and DUF region 170 with respect to reference terminal 102. This increased voltage is capacitively coupled to the enclosed P-well region 171 by means of the parasitic junction capacitance (not shown) of reverse biased diode 186. This increase in voltage serves to forward bias the emitter of the parasitic NPN transistor of MOS transistor 106, thereby initiating conduction of the protection circuit. Alternatively, application of a negative ESD pulse at bond pad 100 will decrease the voltage at lead 110 and forward bias the emitter of the parasitic NPN transistor of MOS transistor 106. Under forward bias, the base current of the parasitic NPN transistor will charge the parasitic junction capacitance (not shown) of reverse biased diode 186. Initial conduction of the protection circuit, therefore, is enhanced by diodes 196 and 198 for either polarity of ESD stress pulse. This is highly advantageous in lowering the trigger threshold of the protection circuit, thereby limiting the maximum voltage at protected circuit 188.

Turning now to FIG. 3, there is a schematic diagram of yet another embodiment of the protection circuit of the present invention. This embodiment is the same as the embodiment of FIG. 1A, except that NPN bipolar transistor 300 replaces MOS transistor 106. This NPN bipolar transistor 300 may be formed by individual N+ regions 180 and 182 without intervening gate region 126 (FIG. 1A). Operation of the protection circuit is the same as previously described for the parasitic NPN transistor of MOS transistor 106 in previous embodiments. A further

advantage of this embodiment, however, is that thin oxide regions are eliminated in the primary protection device. Elimination of these thin oxide regions greatly reduces a likelihood of gate dielectric damage due to rapid ESD transients such as charged device stress.

Although the invention has been described in detail with reference to its preferred embodiments, it is to be understood that this description is by way of example only and is not to be construed in a limiting sense. For example, various combinations of resistors and transistors of the previous embodiments may be combined to provide the advantages of the present invention as will be appreciated by one of ordinary skill in the art having access to the instant specification. In particular, the embodiment of FIG. 3 may readily be combined with diodes 196 and 198 of the embodiment of FIG. 2A. Furthermore, the inventive concept of the present invention may be advantageously extended to many parallel transistors 106 or 300 in a semiconductor body without current hogging.

It is to be further understood that numerous changes in the details of the embodiments of the invention will be apparent to persons of ordinary skill in the art having reference to this description. It is contemplated that such changes and additional embodiments are within the spirit and true scope of the invention as claimed below.

WHAT IS CLAIMED:

1. A structure, comprising:

an external terminal;

a reference terminal;

a first transistor formed on a substrate, the first transistor having a current path coupled between the external terminal and the reference terminal;

a second transistor having a current path coupled between the external terminal and the substrate; and

a third transistor having a current path coupled between the substrate and the reference terminal.

2. A structure as in claim 1, further comprising:

a first resistor coupled between the external terminal and the current path of the second transistor; and

a second resistor coupled between the current path of the third transistor and the reference terminal.

3. A structure as in claim 1, wherein the substrate is a first lightly doped region having a first conductivity type.

4. A structure as in claim 3, further comprising:

a first heavily doped region having a second conductivity type and underlying the substrate and the first transistor; and

a second lightly doped region having the second conductivity type, the second lightly doped region formed at a face of the substrate and extending to the first heavily doped region.

5. A structure as in claim 4, further comprising:

a first diode coupled between the external terminal and the second lightly doped region; and

a second diode coupled between the reference terminal and the second lightly doped region.

6. A structure as in claim 1, wherein the first transistor further comprises a control terminal coupled to the substrate.

7. A structure as in claim 6, further comprising:

a first resistor coupled between the external terminal and the current path of the second transistor; and

a second resistor coupled between the current path of the third transistor and the reference terminal.

8. A structure as in claim 7, wherein the substrate is a first lightly doped region having a first conductivity type, the structure further comprising:

a first heavily doped region having a second conductivity type and underlying the substrate and the first transistor; and

a second lightly doped region having the second conductivity type, the second lightly doped region formed at a face of the substrate and extending to the first heavily doped region.

9. A structure as in claim 8, further comprising:

a first diode having a first terminal coupled to the second lightly doped region and having a second terminal coupled between the first resistor and the current path of the second transistor; and

a second diode having a first terminal coupled to the second lightly doped region and having a second terminal coupled between the second resistor and the current path of the third transistor.

10. A structure as in claim 9, further comprising:

an isolation circuit connected to the external terminal; and

a protected circuit electrically connected to the isolation circuit.

11. A structure as in claim 1, further comprising a protected circuit electrically connected to the external terminal.

12. A structure as in claim 1, wherein the first transistor is an MOS transistor having a control gate coupled to the substrate.

13. A structure as in claim 1, wherein the first transistor is a bipolar transistor having a base terminal coupled to the substrate.

14. A method of forming a circuit, comprising the steps of:

forming a first device having a current path and a control terminal between an external terminal and a reference terminal, the external terminal coupled to receive a maximum positive voltage with respect to the reference terminal and a minimum negative voltage with respect to the reference terminal during normal circuit operation;

forming a second device having a current path connected to the control terminal of the first transistor, the second device arranged to inhibit conduction of the current path of the first device in response to the maximum positive voltage; and

forming a third device having a current path connected to the control terminal of the first transistor, the third device arranged to inhibit conduction of the current path of the first device in response to the minimum negative voltage.

15. A method as in claim 14, further comprising the steps of:

connecting a first resistor between the external terminal and the current path of the second device; and

connecting a second resistor between the current path of the third device and the reference terminal.

16. A method as in claim 14, further comprising the steps of:

forming a first lightly doped region having a first conductivity type and underlying the first device;

forming a first heavily doped region having a second conductivity type and underlying the first lightly doped region; and

forming a second lightly doped region having the second conductivity type, the second lightly doped region extending from a face of the first lightly doped region to the first heavily doped region.

17. A method as in claim 16, further comprising the steps of:

forming a first diode coupled between the external terminal and the second lightly doped region; and

forming a second diode coupled between the reference terminal and the second lightly doped region.

18. A method as in claim 16, further comprising the step of connecting the control terminal of the first device to the first lightly doped region.

19. A method as in claim 18, further comprising the step of connecting a protected circuit to the external circuit.

20. A method as in claim 19, wherein the first device is a bipolar transistor and wherein the first lightly doped region comprises a base terminal of the bipolar transistor.

ABSTRACT

A structure is designed with an external terminal (100) and a reference terminal (102). A first transistor (106) is formed on a substrate. The first transistor has a current path coupled between the external terminal and the reference terminal. A second transistor (118) has a current path coupled between the external terminal and the substrate. A third transistor (120) has a current path coupled between the substrate and the reference terminal.

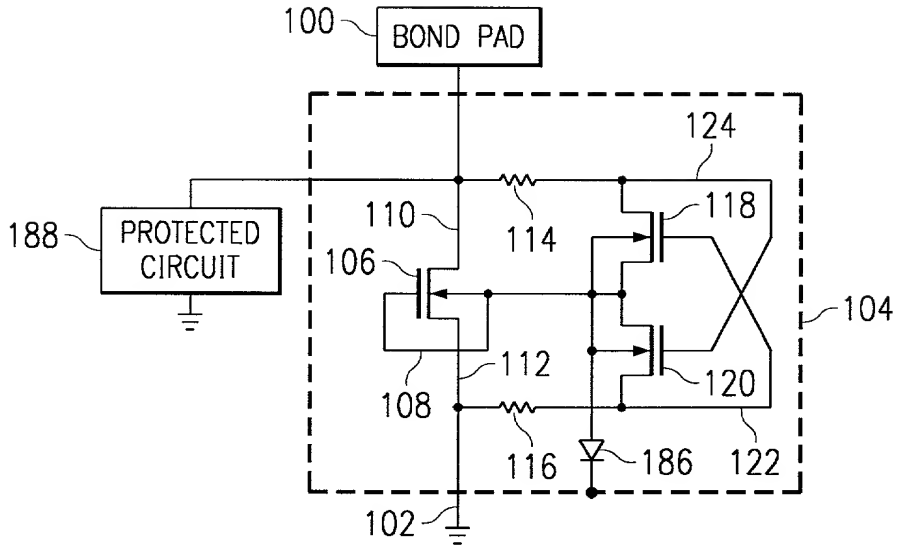
100
BOND PAD
124
188
PROTECTED CIRCUIT
110
114
118
106
104
112
120
108
116
186
122
102

FIG. 1A

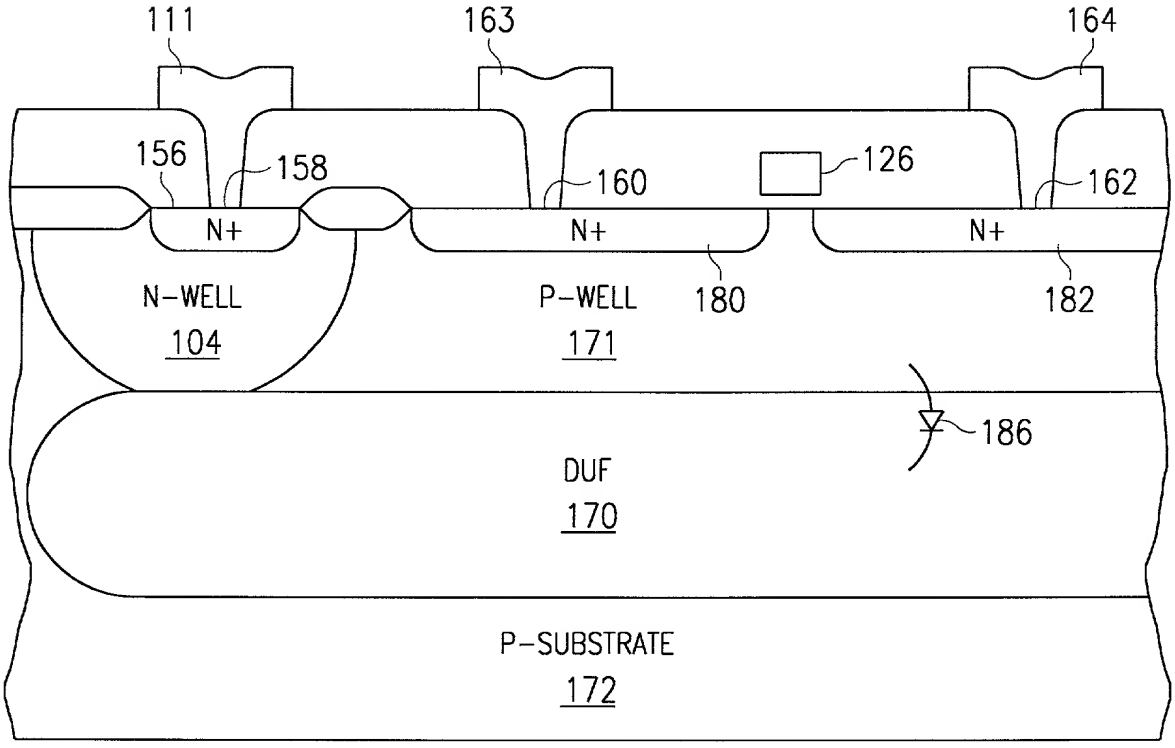
111
163
164
156
158
160
126
162
N+
N+
N+
N-WELL
104
P-WELL
171
180
182
186
DUF
170
P-SUBSTRATE
172

FIG. 1C

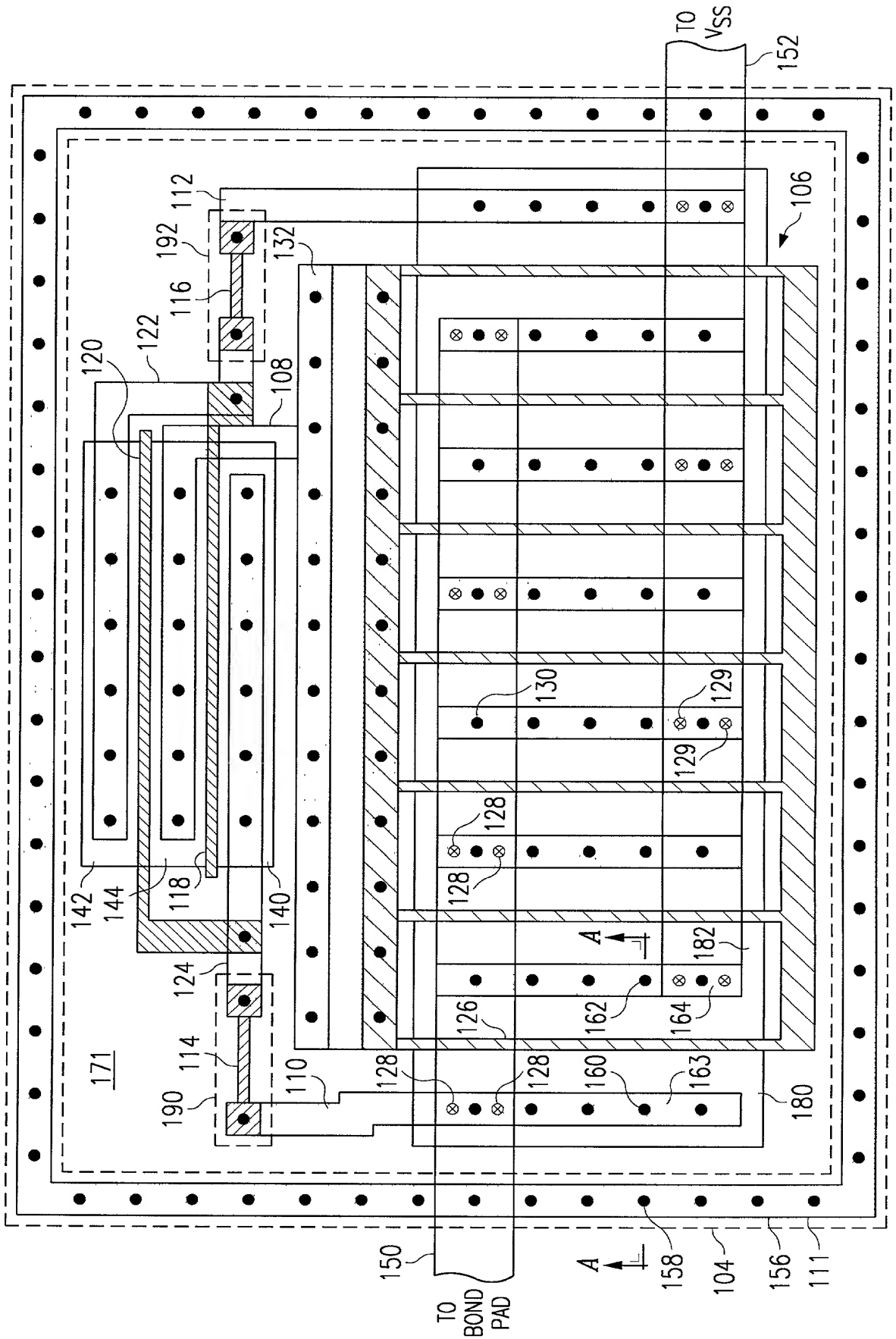
TO V_{SS}
152
106
112
192
116
132
122
120
108
142
144
118
140
124
114
190
110
171
130
129
128
126
162
164
182
160
163
180
A
150
TO BOND PAD
158
104
156
111

FIG. 1B

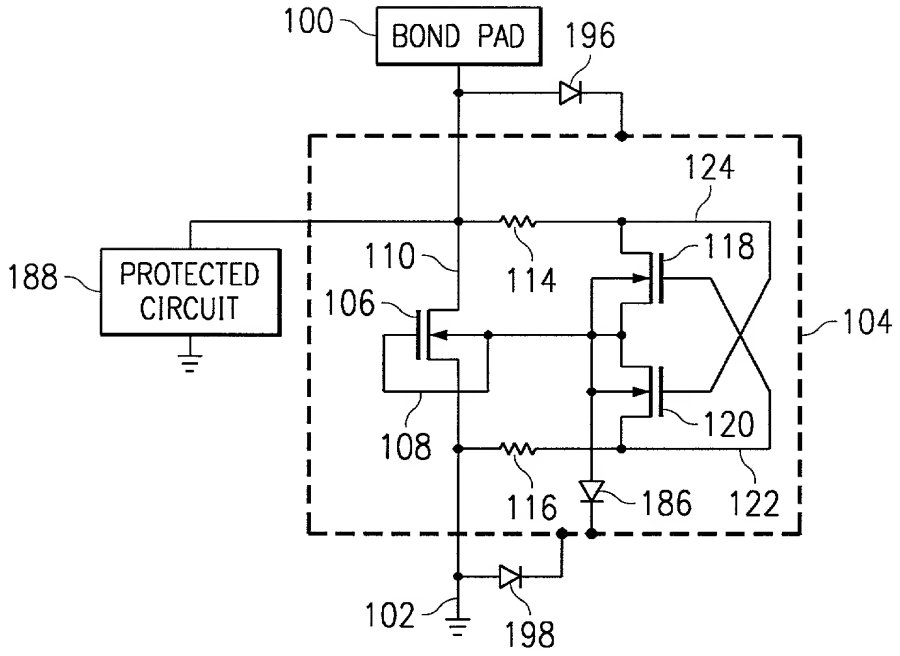

FIG. 2A

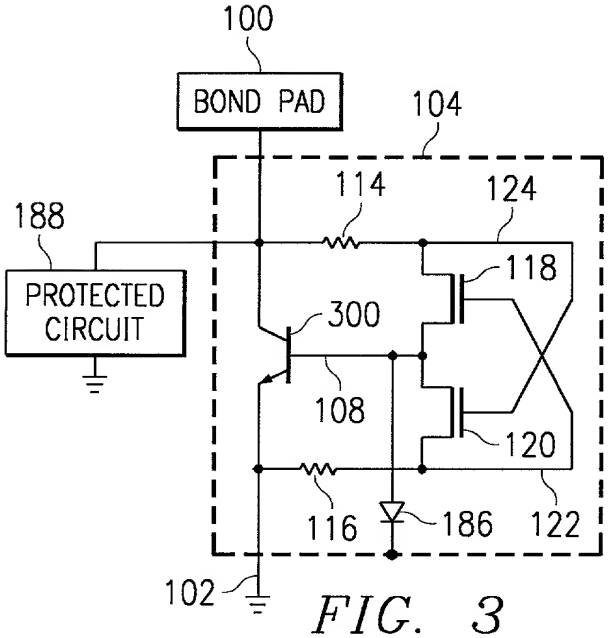

FIG. 3

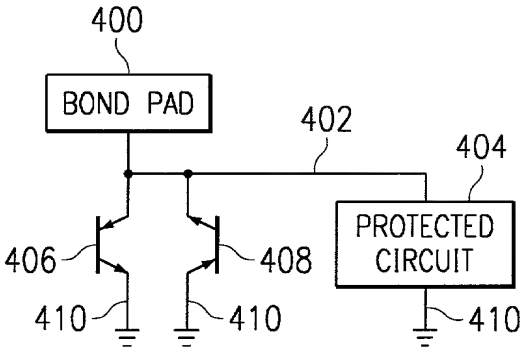

FIG. 4
(PRIOR ART)

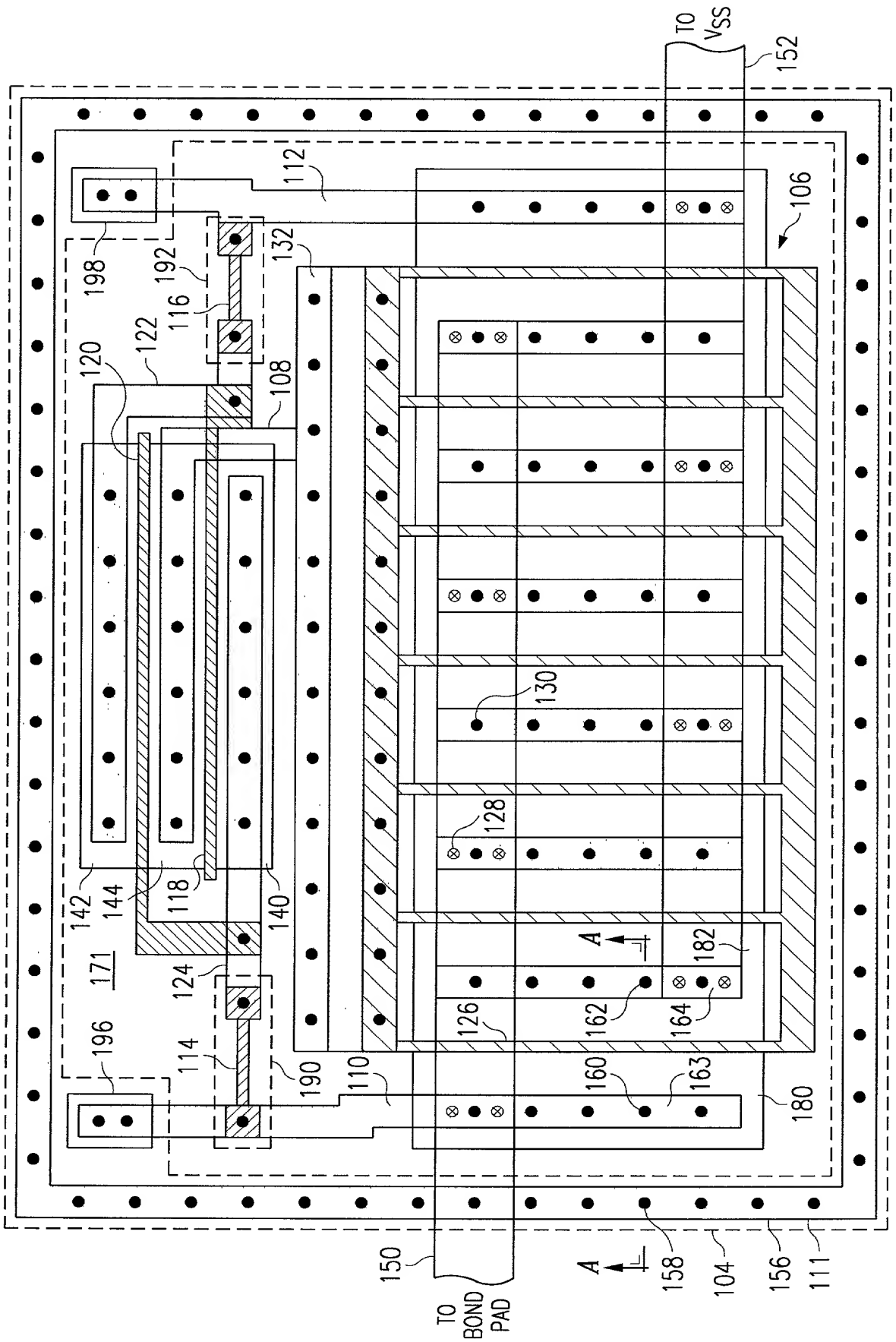
TO V_{SS}
152
112
106
198
192
132
116
122
120
108
130
128
142
144
118
140
171
124
182
A
126
162
164
196
114
190
110
160
163
180
150
TO BOND PAD
158
104
156
111

FIG. 2B

ATTORNEY'S DOCKET NO.
TI – 29599

APPLICATION FOR UNITED STATES PATENT
DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, section 1.56.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION: ***BI-DIRECTIONAL ESD PROTECTION CIRCUIT***		
POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH: ***Robert N. Rountree, Reg. No. 39,347*** ***Jay Cantor, Reg. No. 19,906*** ***Richard L. Donaldson, Reg. No. 25,673*** ***Robby T. Holland, Reg. No. 33,304*** ***William B. Kempler, Reg. No. 28,228*** ***Ronald O. Neerings, Reg. No.: 34,227***		
SEND CORRESPONDENCE TO: ***ROBERT N. ROUNTREE*** ***Texas Instruments Incorporated*** ***P. O. Box 655474, M.S. 3999*** ***Dallas, Texas 75265***		DIRECT TELEPHONE CALLS TO: ***Robert N. Rountree*** ***(972) 917-4431***
NAME OF INVENTOR: (1) ***ROBERT STEINHOFF***	NAME OF INVENTOR: (2) ***JONATHAN S. BRODSKY***	NAME OF INVENTOR: (3) ***THOMAS A. VROTSOS***
RESIDENCE (City and State Only) ***Dallas, Texas***	RESIDENCE (City and State Only) ***Richardson, Texas***	RESIDENCE (City and State Only) ***Plano, Texas***
POST OFFICE ADDRESS ***8285 Southwestern Blvd., Apt. 1101*** ***Dallas, Texas 75206***	POST OFFICE ADDRESS ***800 West Renner Road, Apt. 1923*** ***Richardson, Texas 75080***	POST OFFICE ADDRESS ***1116 Spring View Lane*** ***Plano, Texas 75075***
COUNTRY OF CITIZENSHIP: ***U.S.A.***	COUNTRY OF CITIZENSHIP: ***U.S.A.***	COUNTRY OF CITIZENSHIP: ***U.S.A.***
SIGNATURE OF INVENTOR: X Robert Steinhoff	SIGNATURE OF INVENTOR: Jonathan S. Brodsky	SIGNATURE OF INVENTOR: T. A. Vrotsos
DATE: 2/4/00	DATE: 02-04-2000	DATE: 2-4-00